AN1334
APPLICATION NOTE

ST10F269/F280 System Reset

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1 - INTRODUCTION

This application note is intended for hardware designers. It explains the different kinds of reset available on ST10F269/ST10F280 and compares ST10F269/ST10F280 reset features with ST10F168 ones.

More specifically, after a quick summary, it details the new flags added to WDTCON register, then gives an application view of the different resets. A specific chapter is devoted to the bidirectional reset to detail the advantages and constraints of using this mode.

After describing the start-up configuration, users will find a chapter detailing ST10 reset key parameters.

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2 - SYSTEM RESET

System reset initializes a device into a pre-defined default state.

ST10F269 and ST10F280 have the same types of reset as ST10F168

– Asynchronous hardware reset: defined by assertion of the $\overline{\text{RSTIN}}$ pin with a low level on RPD pin.
– Synchronous short hardware reset: defined by assertion of the $\overline{\text{RSTIN}}$ pin for less 1032 TCL, with a high level on RPD pin.
– Synchronous long hardware reset: defined by assertion of the $\overline{\text{RSTIN}}$ pin more than 1032 TCL, with a high level on RPD pin.
– Software reset: reset initiated by the execution of SRST instruction.
– Watchdog reset: reset triggered by an overflow of the watchdog timer.

The functionalities associated to reset are unchanged

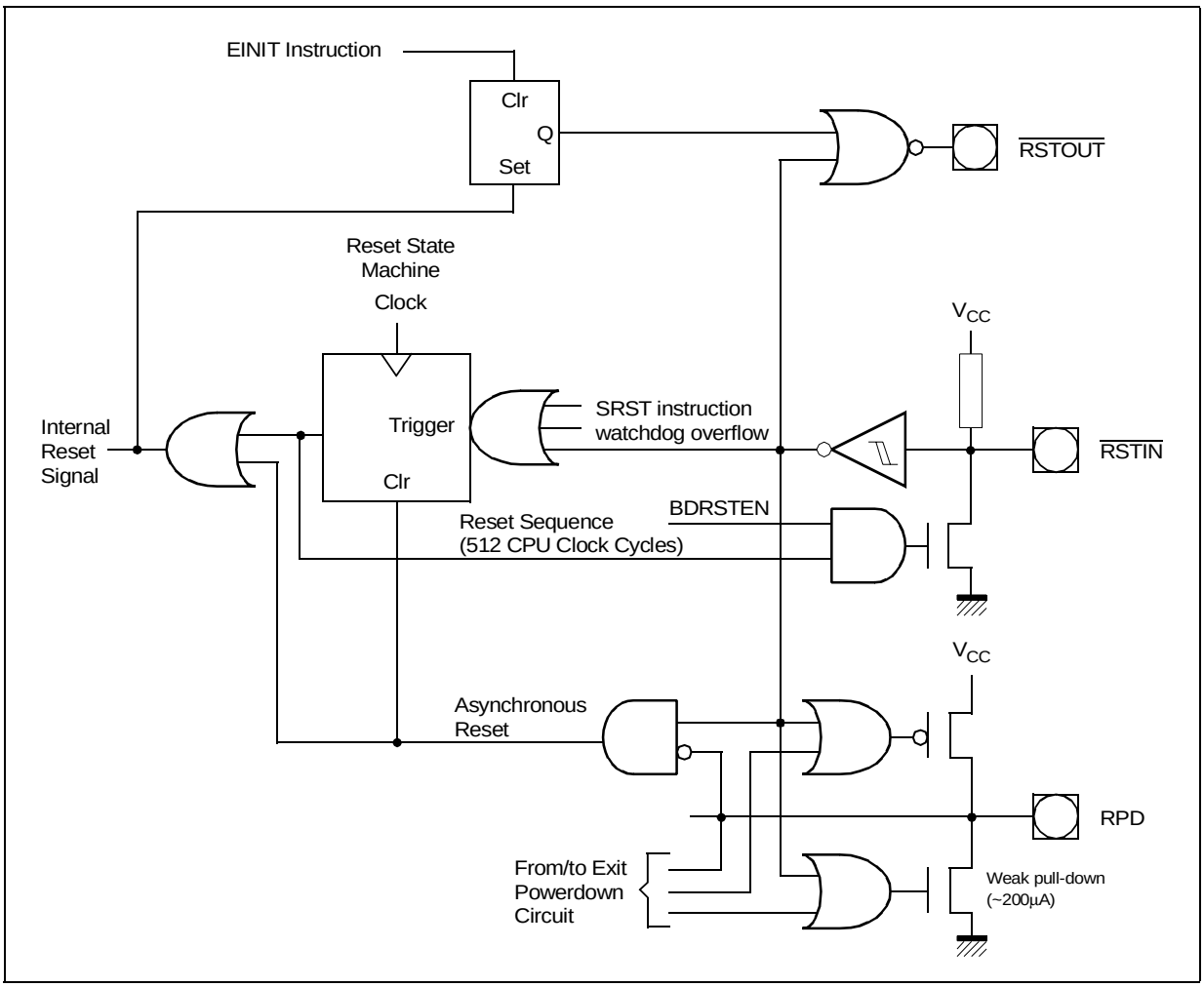
– Bidirectional reset can be enabled to convert software and watchdog resets to hardware reset.
– $\overline{\text{RSTOUT}}$ is activated once reset conditions are detected and remains active until the execution of the EINIT instruction. The CPU and peripherals are set in their predefined default state.
– The content of some special function registers (SYSCON, BUSCON0, RP0H) are controlled during system start-up configuration via PORT0 pins. The system start-up configuration is sampled differently upon the different reset types.
– After the internal reset condition is removed, the microcontroller will start program execution from memory location 00’0000h in code segment zero. This start location will typically hold a branch instruction to the start of a software initialization routine for the application specific configuration of peripherals and CPU Special Function Registers.

Difference with ST10F168

The main difference with ST10F168 is that register WDTCON has been modified to support 1 flag per reset source to indicate the reset cause.

ST10F269 and ST10F280 internal reset circuitry is the following:

Figure 1 : Internal Reset Circuitry



Note: ST10F269 and ST10F280 internal reset circuitry is the same as ST10F168 except that VPP pin is used only for the timing control during "Return from Powerdown" and to select the type of reset: asynchronous or synchronous type of reset. Pin 84 name is now "RPD" .

3 - WDTCON NEW FLAGS FOR RESET CAUSES

3.1 - WDTCON Description

Compared to ST10F168, ST10F269 and ST10F280 WDTCON registers have been modified to indicate the cause of the reset:

Each of the different reset sources is now indicated in the WDTCON register. The indicated bits are cleared with the EINIT instruction. It is thus possible to identify the reset during the initialisation phase.

WDTCON (FFAEh / D7h) SFR Reset Value: 00XXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTREL								-	-	PONR	LHWR	SHWR	SWR	WDTR	WDTIN
RW										HR	HR	HR	HR	HR	RW

WDTIN	**Watchdog Timer Input Frequency Selection** '0': Input Frequency is $f_{CPU}/2$. '1': Input Frequency is $f_{CPU}/128$.
WDTR [1 - 3]	**Watchdog Timer Reset Indication Flag** Set by the watchdog timer on an overflow. Cleared by a hardware reset or by the SRVWDT instruction.
SWR [1-3]	**Software Reset Indication Flag** Set by the SRST execution. Cleared by the EINIT instruction.
SHWR [1-3]	**Short Hardware Reset Indication Flag** Set by the input $\overline{\text{RSTIN}}$. Cleared by the EINIT instruction.
LHWR [1-3]	**Long Hardware Reset Indication Flag** Set by the input $\overline{\text{RSTIN}}$. Cleared by the EINIT instruction.
PONR [1- 2-3]	**Power-On (Asynchronous) Reset Indication Flag** Set by the input $\overline{\text{RSTIN}}$ if a power-on condition has been detected. Cleared by the EINIT instruction.

Notes: 1. More than one reset indication flag may be set. After EINIT, all flags are cleared.
2. Power-on is detected when a rising edge from Vcc = 0V to Vcc > 2.0V is recognized on the internal 3.3V supply.
3. Those bits cannot be directly modified by software...

3.2 - Power-on Detection

ST10F269 and ST10F280 have power-on detection circuitry.

The PONR flag of WDTCON register is set if the output voltage of the internal 3.3V supply falls below the threshold (typically 2V) of the power-on detection circuit. This circuit is efficient to detect major failures of the external 5V supply but if the internal 3.3V supply does not drop under 2 volts, the PONR flag is not set. This could be the case on fast switch-off / switch-on of the 5V supply. The time needed for such a sequence to activate the PONR flag depends on the value of the capacitors connected to the supply and on the exact value of the internal threshold of the detection circuit.

3.3 - Supply Monitoring

ST10F269 and ST10F280 have on-chip power-on detection circuitry. This circuitry is detecting major failure on the supply and will not generate a reset when the external supply is going out of ST10 circuit specification (either marginally, either for a very short period).

As a consequence, when an external supply monitoring circuit is used, the table of WDTCON after reset becomes:

The following table is showing the value of WDTCON bits for the 6 possible causes of reset:

Reset Source	PONR	LHWR	SHWR	SWR	WDTR
Power-on Reset (all bit are set)	X	X	X	X	
Power-on after Partial Supply Failure	*	X	X	X	
Long Hardware Reset		X	X	X	
Short Hardware Reset			X	X	
Software Reset (only SWR bit is set)				X	
Watchdog Reset				X	X

** PONR bit may not be set for short supply failure.*
For Power on reset after supply partial failure, asynchronous reset must be used.
In case bi-directional reset is enabled, and if the RSTIN pin is latched low after the end of internal reset sequence, then a Short hardware reset, a software reset or a watchdog reset will trigger a Long hardware reset. Thus, Reset Indications flags will be set to indicate a Long Hardware Reset.

4 - RSTOUT PIN

The behaviour or RSTOUT pin of ST10F269 and ST10F280 is identical to ST10168:

The RSTOUT pin is dedicated to generate a reset signal for the system components besides the controller itself.

RSTOUT pin is activated once reset conditions are detected.

For synchronous reset, as the CPU is completing its current bus cycle, RSTOUT may be activated before the internal CPU reset sequence is started.

RSTOUT remains activated until the execution of the EINIT instruction. This allows the complete configuration of the controller including its on-chip peripheral units before releasing the reset signal for the external peripherals of the system.

RSTOUT will float as long as pins P0L.0 and POL.1 select emulation mode or adapt mode; to avoid pulses on RSTOUT P0L.0 and P0L.1 are latched at the end of the reset sequence (see diagrams showing sampling point of PORT0 pins).

5 - RESET AND RPD PIN

As explained before, the level on pin RPD (pin 84) defines the reset type when RSTIN is activated:

– Asynchronous reset: defined by assertion of the RSTIN pin with a low level on RPD pin.

– Synchronous reset: defined by assertion of the RSTIN pin with a high level on RPD pin.

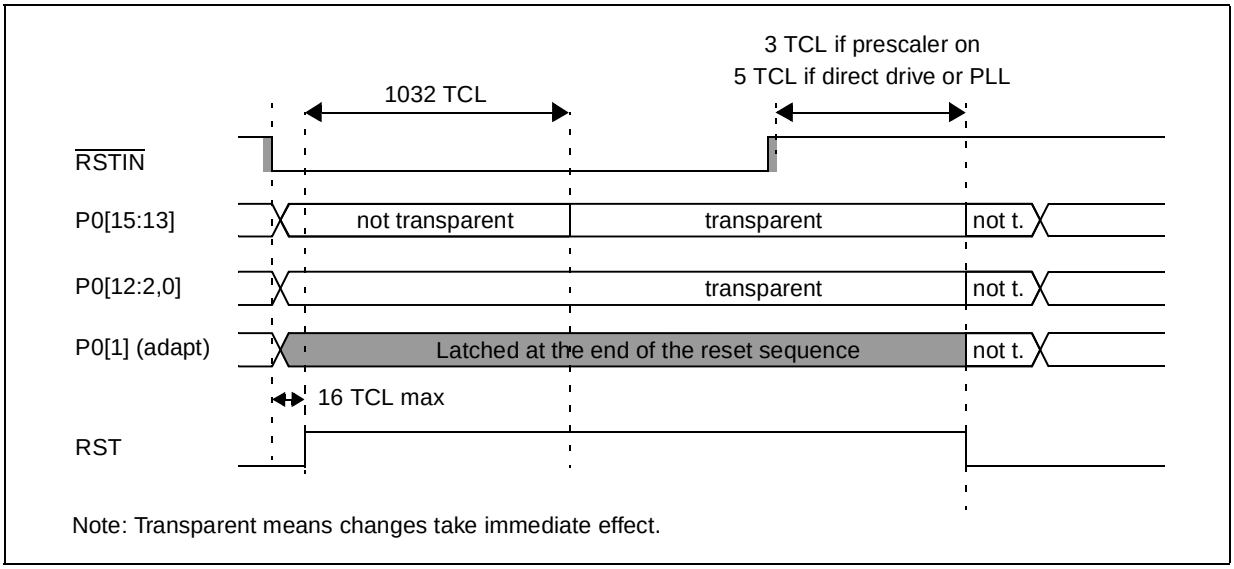
Then, if RPD is pulled low in synchronous reset, the chip immediatly enters in asynchronous reset.

Synchronous Reset

Advantage: this reset shall be used when short pulses on RSTIN pin can be applied to generate a circuit reset during circuit operation.

Disadvantage: reset effect on circuit may be delayed up to 2 CPU clock cycles (sampling time) and then by another period to leave the CPU to complete the current internal bus cycle.

Figure 2 : Long Synchronous Reset Sequence



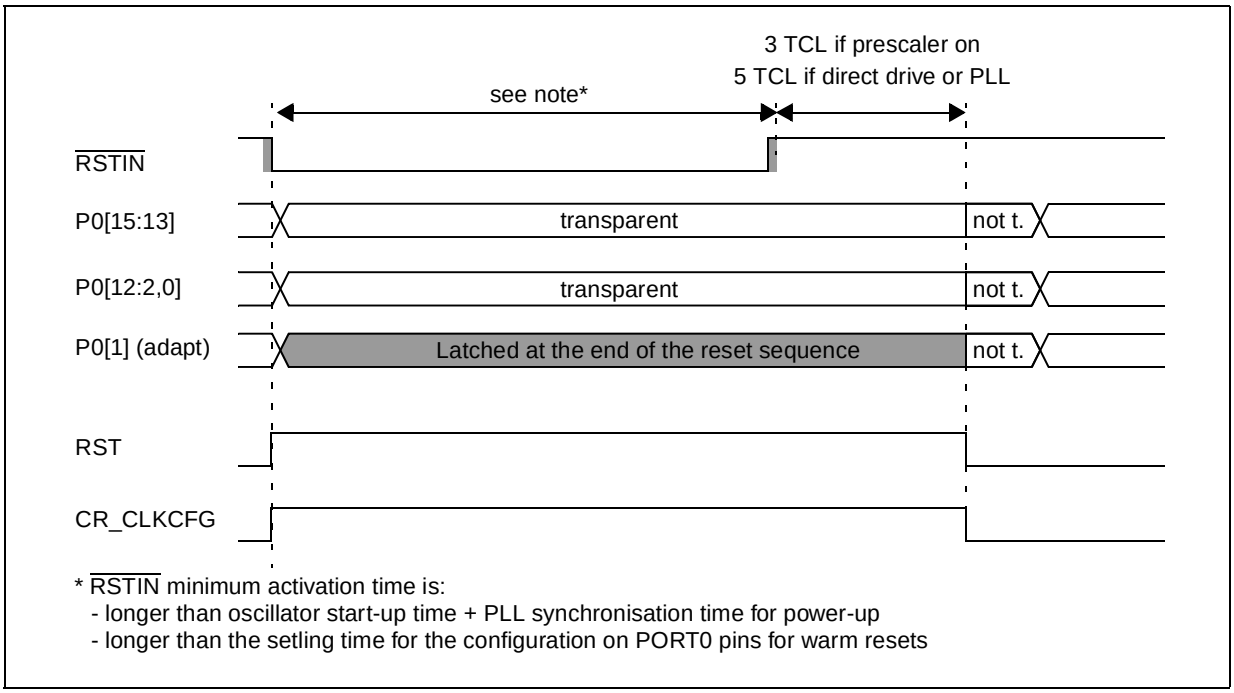
Asynchronous Reset

Advantage: $\overline{\text{RSTIN}}$ has an immediate (asynchronous) effect on the circuit.

Disadvantage: $\overline{\text{RSTIN}}$ must be held low for the whole duration of the circuit internal reset sequence; if not, the circuit may enter in endless undefined state.

This reset shall be used upon power-up.

Figure 3 : Asynchronous Reset Sequence



6 - APPLICATION VIEW

From application standpoint, there are 6 causes to system reset. The system start-up configuration is different for each:

Table 1 : ST10F269/F280 Reset Causes

Reset Source	Short-cut	Condition
Power-on reset	PONR	Power-on
Power-on after partial power failure	POAF	Power-on with supply not ramping up from 0V
Short Hardware reset	SHWR	4 TCL < t_{RSTIN} ≤ 1032 TCL
Long Hardware reset	LHWR	t_{RSTIN} > 1032 TCL
Watchdog timer reset	WDTR	WDT overflow
Software reset	SWR	SRST execution

6.1 - Power-on Hardware Reset

Definition: Reset generated upon supply ramp-up from 0V.

Type of Reset to Use: Asynchronous reset must be used.

Flags activated in WDTCON Register: PONR, LHWR, SHWR, SWR.

A power-on reset requires RPD to be held low and $\overline{\text{RSTIN}}$ to be held active (low) till a stable clock signal is available and till the PLL is stabilised.

Depending on the oscillation frequency, the on-chip oscillator needs 2...50ms to stabilize.

The input $\overline{\text{RSTIN}}$ provides an internal pull-up device equalling a resistor of 50KΩ to 250KΩ (the minimum reset time must be determined by the lowest value). Simply connecting an external capacitor on $\overline{\text{RSTIN}}$ pin is sufficient for an automatic power-on reset.

Chronograms: See respective chronogram in the previous chapter.

6.2 - Power-on Reset After a Partial Power Failure

Definition: Reset generated upon supply ramp-up with the supply ramping from a value higher than 0V.

Type of Reset to Use: Asynchronous reset must be used.

Flags activated in WDTCON Register: LHWR, SHWR, SWR, PONR flag is undefined as its value depend on the voltage remaining on the supply at power-ON. The threshold for ST10F269 and ST10F280 is about 2V.

A power-on reset requires RPD to be held low and $\overline{\text{RSTIN}}$ to be held active (low) still a stable clock signal is available and till the PLL is stabilised.

Depending on the oscillation frequency, the on-chip oscillator needs 2 ... 50ms to stabilize.

The input $\overline{\text{RSTIN}}$ provides an internal pull-up device equalling a resistor of 50KΩ to 250KΩ (the minimum reset time must be determined by the lowest value). Simply connecting an external capacitor on $\overline{\text{RSTIN}}$ pin is sufficient for an automatic power-reset.

Chronograms: See respective chronogram in the previous chapter.

6.3 - Long Hardware Reset

Definition: Hardware reset long enough for the oscillator to re-start and the PLL to re-synchronize while supply is already ON.

Type of Reset to Use: Asynchronous reset or synchronous reset can be used.

Flags activated in WDTCON Register: LHWR, SHWR, SWR

$\overline{\text{RSTIN}}$ signal must be longer than 1032 TCL and longer than 1ms.

A long hardware reset is triggered when the $\overline{\text{RSTIN}}$ signal is held active (low) for at least 1032TCL (20.64µs @ 25MHz CPU clock).

Long hardware reset cancels pending internal hold states, waits for any internal access cycles to finish, aborts external bus cycles, switches off bus pin drivers and I/O pin drivers (tristate), and internally pulls high PORT0 pins. Then, the internal reset sequences starts.

When the internal reset sequence is complete and $\overline{\text{RSTIN}}$ is inactive (i.e. the internal reset condition is removed) the reset configuration is latched from PORT0, and pins ALE, RD and WR driven to their inactive levels. The microcontroller starts program execution from memory location 00'0000h in code segment zero. This start location typically holds a branch instruction to the start of a software initialization routine for the application specific configuration of peripherals and CPU Special Function Registers.

Chronograms: See respective chronogram in the previous chapter.

Note: All PORT0 bits are sampled at the end of a Long Hardware reset to relatch the complete system start-up configuration. As the PLL may temporarily try to run with an interim configuration read on the Port0 pins, you are recommended to keep $\overline{\text{RSTIN}}$ low for approximately 1ms to guarantee that the PLL will be correctly locked.

6.4 - Short Hardware Reset

Definition: Hardware reset generated to restart software from the beginning. Reset pulse is intentionally short so that ST10 can resume operation very quickly. Supply must already be ON.

Type of Reset to Use: Synchronous reset must be used (RPD is high).

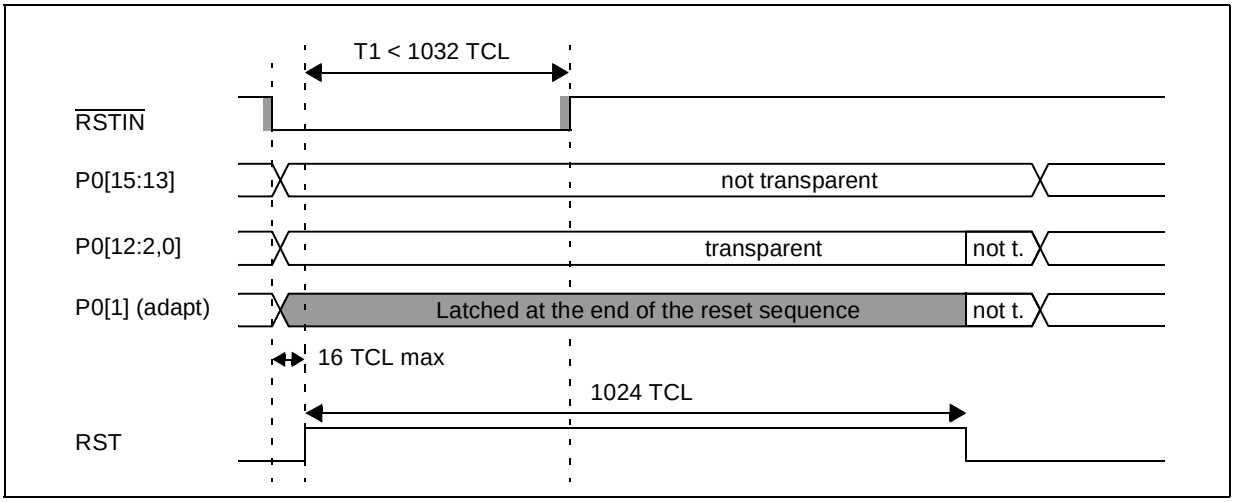
Flags activated in WDTCON Register: SHWR, SWR.

$\overline{\text{RSTIN}}$ signal must be shorter than 1032 TCL and longer than 4 TCL.

A short hardware reset is triggered when the $\overline{\text{RSTIN}}$ signal is held active (low) for more than 4 and less than 1032 TCL (80ns -20.64µs at 25MHz CPU clock). In short hardware reset bits P0.15..P0.13 are not latched at the end of the internal reset condition, therefore the previous PLL configuration is not changed. Otherwise short hardware reset is the same as long hardware reset.

Note: As the ST10 internal reset sequence is short, this reset is not suitable for all situations: the oscillator must be running and the PLL must be already locked before such a reset.

Figure 4 : Short Hardware Synchronous Reset Sequence



6.5 - Software Reset

Definition: Reset initiated by SRST instruction.

Type of Reset to Use: SRST instruction.

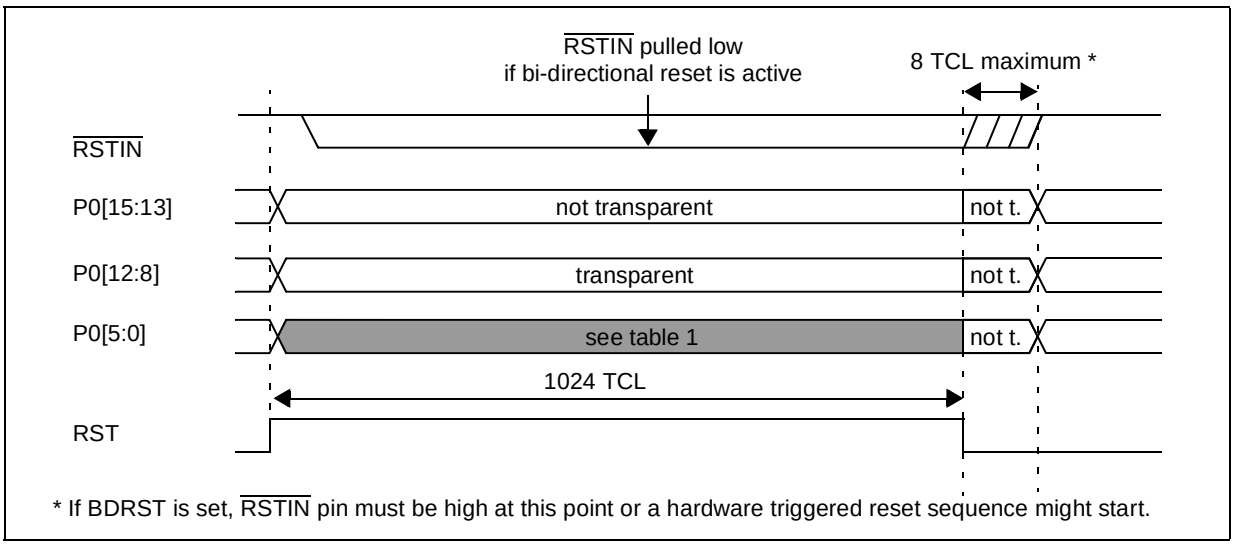
Flags activated in WDTCON Register: SWR.

The level on RPD pin has no effect as long BDRSTEN is not set.

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behaviour is the same as for a short hardware reset, except that only bits P0.12...P0.6 are latched at the end of the reset sequence, while previously latched bits P0.7...P0.2 are cleared.

Figure 5 : Reset Sequence for Software Reset



6.6 - Watchdog Timer Reset

Definition: Reset initiated by the watchdog timer.

Type of Reset to Use: Watchdog time out.

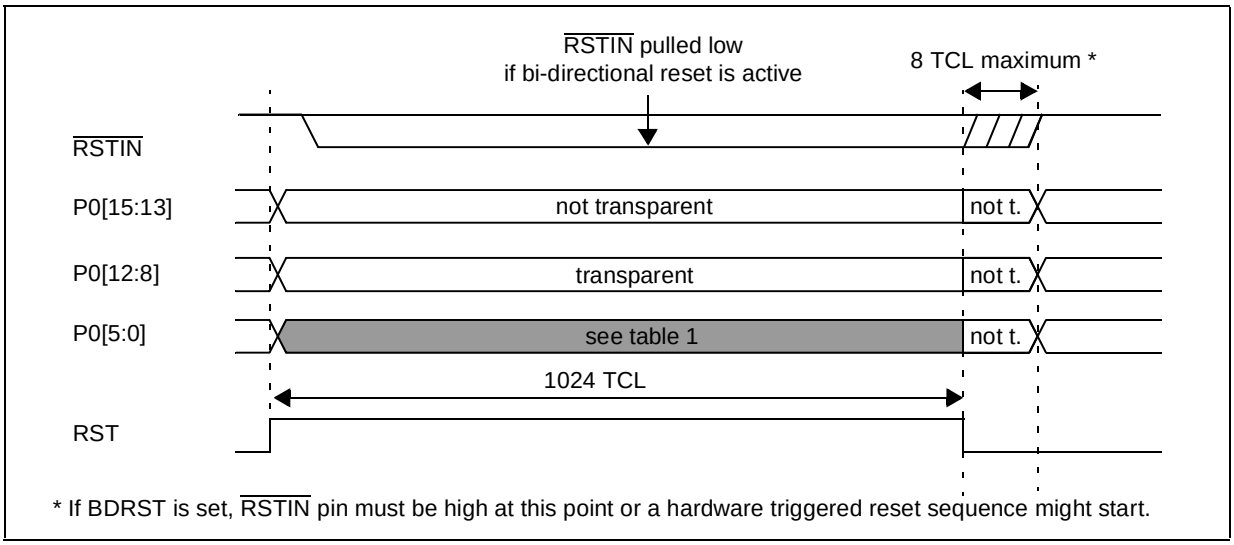
Flags activated in WDTCON Register: WDTR.

The level on RPD pin has no effect as long BDRSTEN is not set.

When the watchdog timer is not disabled during the initialization, or serviced regularly during program execution, it will overflow and trigger the reset sequence. Watchdog reset completes a running external bus cycle if this bus cycle does not use $\overline{\text{READY}}$, or if READY is sampled active (low) after the programmed wait-states. When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed wait-states the running external bus cycle is aborted. Then the internal reset sequence is started.

Bits P0.12...P0.8 are latched at the end of the reset sequence and bits P0.7...P0.2 are cleared.

Figure 6 : Reset Sequence for Watchdog Reset



7 - BI-DIRECTIONAL RESET

Bi-directional reset can be used.

– To convert SW or WDT resets to hardware reset, so that a new configuration can be re-latched,

– To make visible SW or WDT resets at $\overline{\text{RSTIN}}$ pin whenever $\overline{\text{RSTIN}}$ is the only reset signal used by the application ($\overline{\text{RSTOUT}}$ not used),

– To have a $\overline{\text{RSTOUT}}$ signal that is de-activated before the CPU is starting its first instruction fetch.

Converting a SW or WDT reset to a hardware reset allows the PLL to be re-locked or the PLL configuration to be relatched. For some applications, this allows to recover from PLL unlock or input clock fail (provided a SW or WDT reset is generated by the application program in case of PLL unlock or input clock fail and provided the duration of the reset sequence is long enough).

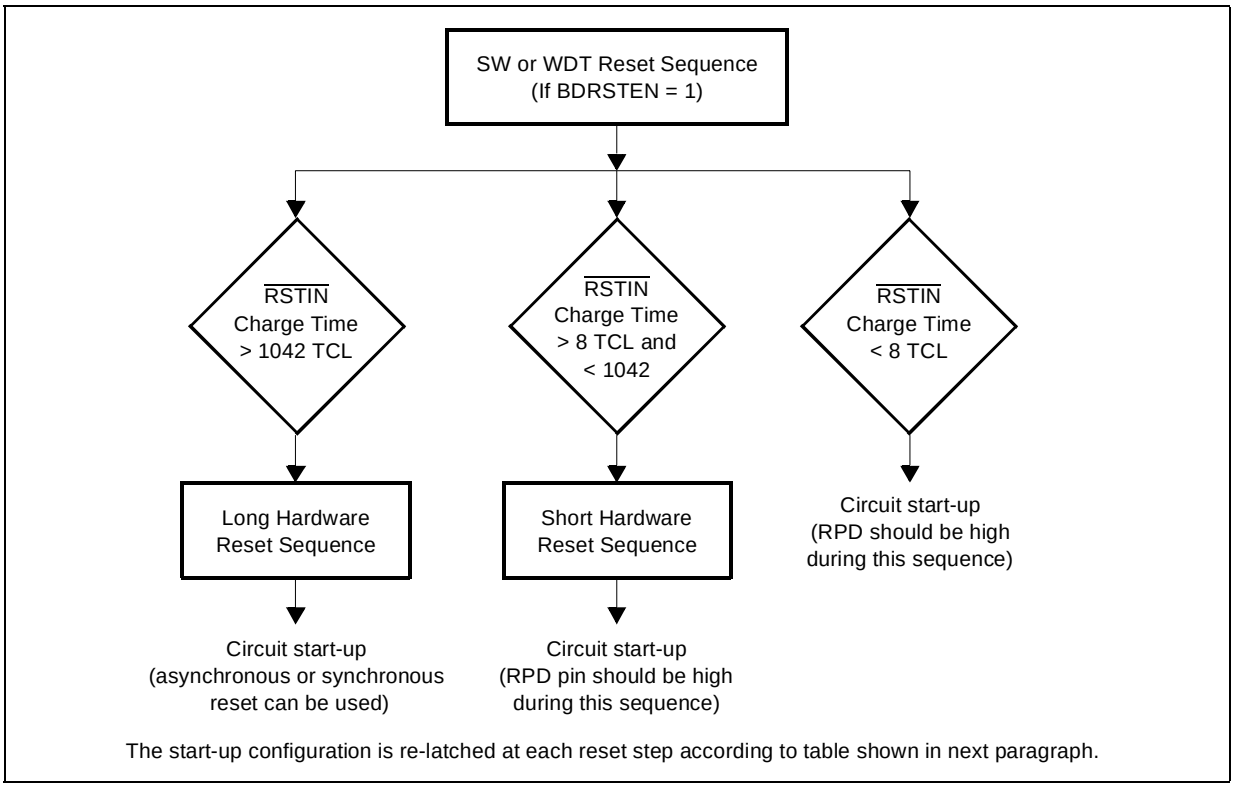
Using bi-directional reset to output a "Reset" signal (at $\overline{\text{RSTIN}}$ pin) that is de-activated before the CPU is starting its first instruction fetch is sometimes mandatory with peripheral having on-chip memory.

When bi-directional reset is enabled, the type of hardware reset generated on SW or WDT depends on the level on RPD pin and on the timing at $\overline{\text{RSTIN}}$ pin.

7.1 - Bi-directional Reset and $\overline{\text{RSTIN}}$ Charge Time

The duration of the rising time on $\overline{\text{RSTIN}}$ pin, defines the type of hardware reset that will be generated and which bits of Port0 will be relatched for the new configuration:

Figure 7 : Reset Sequence for Watchdog Reset



Bi-directional reset is disabled during and after hardware reset and is enabled by setting BDRSTEN bit 3 of the SYSCON register. In bi-directional reset mode, the $\overline{\text{RSTIN}}$ pin is pulled low for the duration of the internal reset sequence.

The bidirectional reset is activating $\overline{\text{RSTIN}}$ pin for the duration of the internal reset sequences caused by a WDT reset or a SW Reset (1024 TCL).

The principle of the hardware implementation is shown in Figure 8. The PORT0 sample timing in case of a bi-directional reset depends on the $\overline{\text{RSTIN}}$ pin charge time (Figure 7).

1. After the execution ot the EINIT instruction the bidirectional reset configuration can not be changed.

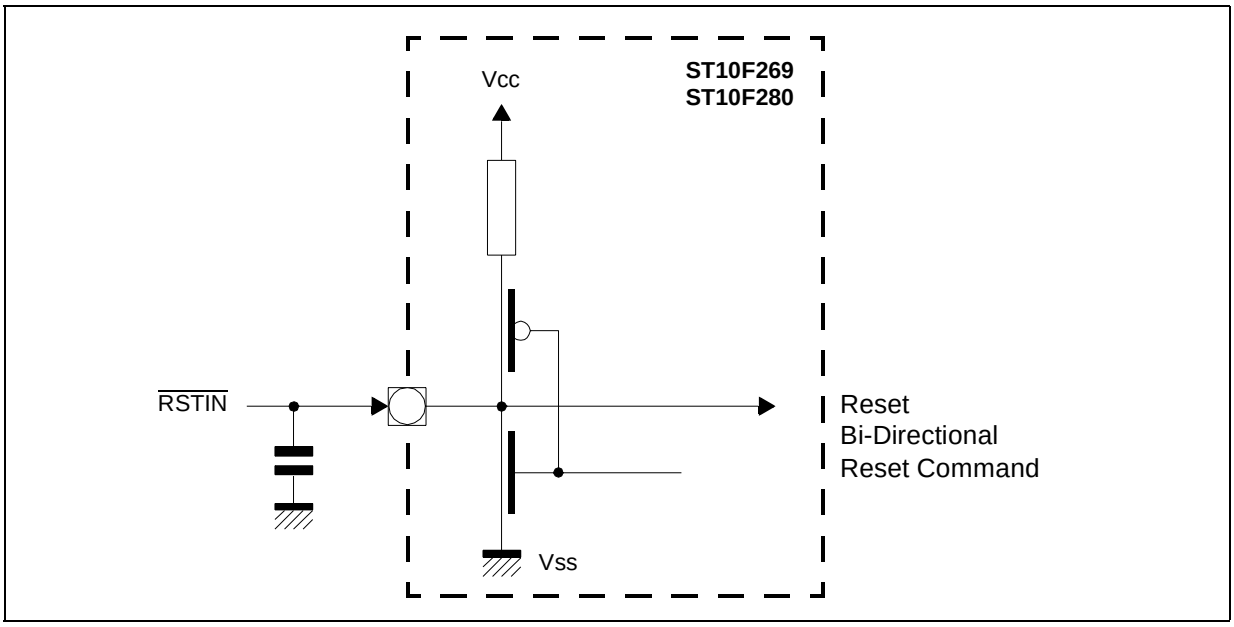
2. WDTCON bit 1 of the WDTR register is cleared after a hardware reset.

3. The bootstrap loader can be started by a WDT reset or SW Reset if the bi-directional reset is enabled and P0L.4 is low and if the $\overline{\text{RSTIN}}$ pin charge time is longer than 8 TCL.

4. If bi-directional reset is enabled then the $\overline{\text{RSTIN}}$ pin may only be connected to external reset devices with an open drain output driver. A connection to a push / pull output driver can damage the $\overline{\text{RSTIN}}$ input.

5. If RPD is low, then the reset sequence may not be long enough for the configuration on Port0 to be stabilized and a wrong configuration may be latched; also, the reset sequence should be long enough to be sure that the oscillator is running and the PLL is stabilised. **RPD low and BDRSTEN = 1 combination shall be carefully handled**.

Figure 8 : Bi-directional Reset: Principle of Hardware Implementation



7.2 - Bi-directional Reset and Short Hardware Reset

The bi-directional reset may affect the behaviour of short hardware resets. This depends on $\overline{\text{RSTIN}}$ charge time:

– Charge time < 8 TCL: the short hardware reset is unchanged.

– Charge time > 8 TCL: the short hardware reset is converted in a long hardware reset (see Figure 7 and Table 1 to check the new configuration latching).

8 - SYSTEM START-UP CONFIGURATION

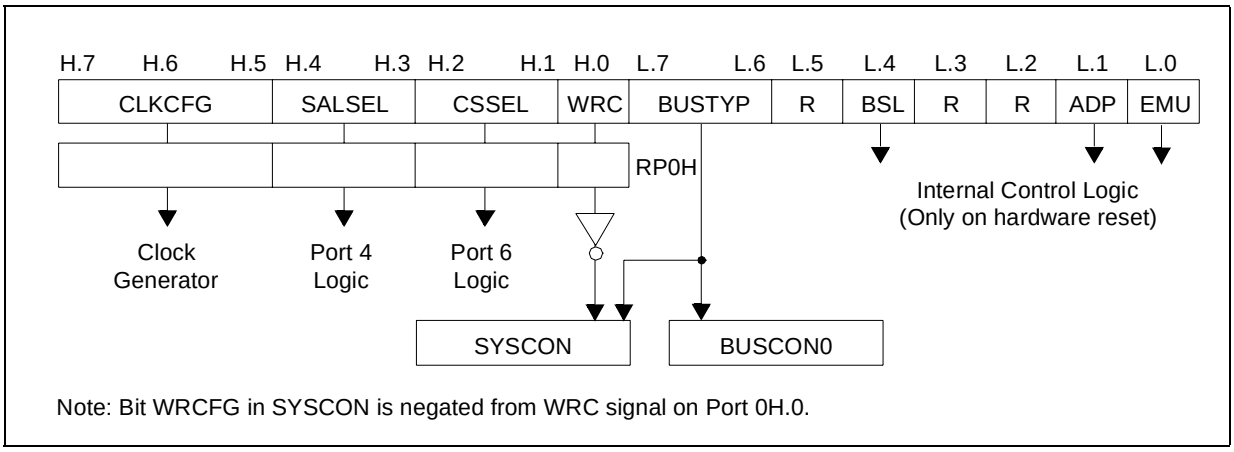
Although most programmable features are either selected during the initialization phase or repeatedly during program execution, there are some features that must be selected earlier because they are used for the first access of the program execution (e.g. internal or external start selected via $\overline{\text{EA}}$).

These selections are made during reset by the pins of PORT0 which are read at the end of the internal reset sequence. During reset, internal pull-up devices are active on the PORT0 lines so their input level is high, if the respective pin is left open or is low, or if the respective pin is connected to an external pull-down device. With the coding of the selections, as shown below, in many cases the default option, i.e. high level, can be used.

The value on the upper byte of PORT0 (P0H) is latched into register RP0H upon reset, the value on the lower byte (P0L) directly influences the BUSCON0 register (bus mode) or the internal control logic of the ST10F269/ST10F280.

Not all Port0 bits are latched after then end of an internal reset. Depending on the reset type, different bits are latched. When $\overline{\text{RSTIN}}$ goes active, some PORT0 configuration input pins are not transparent for the first 1024 TCL. After that time only, these pins are transparent and will be latched when internal reset signal becomes inactive (see Figures 2 to 6). To avoid unexpected behavior, the level of the PORT0 configuration input pins should not change while PORT0 is transparent).

Figure 9 : Port0 Configuration During Reset



Note: Bit WRCFG in SYSCON is negated from WRC signal on Port 0H.0.

Table 2 : Port0 Configuration During Reset

X : Pin is sampled **- : Pin is not sampled** **i : Set inactive**	**PORT0**															
	Clock Options			**Segm. Addr. Lines**		**Chip Selects**		**WR config.**	**Bus Type**		**Reserved**	**BSL**	**Reserved**	**Reserved**	**Adapt Mode**	**Emu Mode**
Sample event	**P0H.7**	**P0H.6**	**P0H.5**	**P0H.4**	**P0H.3**	**P0H.2**	**P0H.1**	**P0H.0**	**P0L.7**	**P0L.6**	**P0L.5**	**P0L.4**	**P0L.3**	**P0L.2**	**P0L.1**	**P0L.0**
Software Reset	-	-	-	X	X	X	X	X	X	X	-	i	-	-	-	-
Watchdog Reset	-	-	-	X	X	X	X	X	X	X	-	i	-	-	-	-
Short Hardware Reset (RPD = "1")	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X
Long Hardware Reset (RPD = "0" or RPD = "1")	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Power-On Reset or Power-ON after partial supply failure (RPD = "0")	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Notes: 1. The bi-directional reset functionality has no impact on the system start-up configuration latching.

2. If the PLL factor or the input clock frequency is changed when PORT0 is transparent, then the PLL needs a PLL synchronization lock time (typical value is 500µs).

The pins that control the operation of the internal control logic and the reserved pins are evaluated only during a hardware triggered reset sequence. The pins that influence the configuration of the ST10F269 / ST10F280 are evaluated during any reset sequence, i.e. also during software and watchdog timer triggered resets.

The configuration via P0H is latched in register RP0H for subsequent evaluation by software. Register RP0H is described in chapter "The External Bus Interface".

Note: The reserved pins (marked "**R**") must remain high during reset in order to ensure proper operation of the ST10F269 / ST10F280. The load on those pins must be small enough for the internal pull-up device to keep their level high, or external pull-up devices must ensure the high level.

9 - RESET KEY PARAMETERS

Reset key parameters are:

– $\overline{\text{RSTIN}}$ activation time,

– Value of configuration resistors on Port0,

– Type and value of components connected on RPD pin.

9.1 - $\overline{\text{RSTIN}}$ Activation Time

9.1.1 - Power-on Reset Time

Power-on reset time should be long enough for the oscillator to start-up and stabilize (typ.: 10.. 50ms check your worse case start-up time).

9.1.2 - Asynchronous Reset

Reset active minimum time should be longer than the oscillator start-up time and PLL synchronisation time.

9.1.3 - Software or Watchdog Reset

When bi-directional reset is enabled, reset active time defines the type of failure that can be recovered from:

– PLL unlock: 1ms minimum for PLL re-lock sequence (once external clock is stabilised)

– Input clock: 10 to 50ms (typically) for oscillator start-up time

The input $\overline{\text{RSTIN}}$ provides an internal pull-up device equalling a resistor of 50KΩ to 15KΩ. Check your application worse cases against latest data sheet values.

9.2 - Configuration Resistors on Port0

Configuration resistors shall be defined so that the input voltage on pins to be latched is within data sheet input voltage specification at the time those pins are latched.

9.2.1 - Pull-down Resistors

Pull-down resistors shall be low enough so that input voltage in P0.x is within circuit specification when taking into account the circuit pull-up current (see PORT0 configuration current for Vin = VILmax) and other leakage currents from external circuits connected to PORT0 pins.

– Formula: $Rpd < (VILmax) / (I_{P0L} + I_{other_circuits})$

– Recommended maximum value: Rpd = 8KΩ. (no other circuit)

9.2.2 - Pull-up Resistors

As mentionned, PORT0 supplies internal pull-up resistors which are active during reset. Pull-up resistors shall be low enough so that input voltage in P0.x is within circuit specification when taking into account the circuit pull-up current (see PORT0 configuration current for Vin = VIHmin) and other leakage currents from external circuits connected to PORT0 pins. For worse case evaluation, leakage current from other external circuits shall always be added to circuit leakage current).

– Formula: $Rpu < (VCCmin - VIHmin) / (I_{other_circuits} - I_{POH})$

– No external pull-up resistor necessary if $I_{other_circuits} - I_{POH}$

9.2.3 - PLL Lock Sequence, Configuration Resistors and Reset Duration

When clock configuration is to be latched, the input voltage on P0H.7..P0H.5 shall not change from the time PORT0 is transparent.

If the input voltage on P0H.7..P0H.5 are not stabilised at this time, then reset duration shall be checked to leave time for the PLL to lock, 1ms typically.

9.3 - Components on RPD Pin

9.3.1 - Difference with ST10F168

The main difference with ST10F168 is that pin 84 has now only 2 functions:

– To define the timing for the return from power-down,

– To define the type of hardware reset.

As a consequence, the components on pin 84 only depends if interruptible power-down mode is used or not used.

9.3.2 - Interruptible Power-down Mode Not Used

RPD shall be tied to GND via a pull-down resistor (1MΩ max.) to ensure asynchronous reset is generated upon power-up.

9.3.3 - Interruptible Mode is Used

A capacitor has to be connected to the RPD pin to generate a delay to allow the oscillator and PLL to resume and stabilise before the internal CPU and peripheral clocks are enabled. Then, a pull-up resistor has to be connected to avoid the discharge of the capacitor.

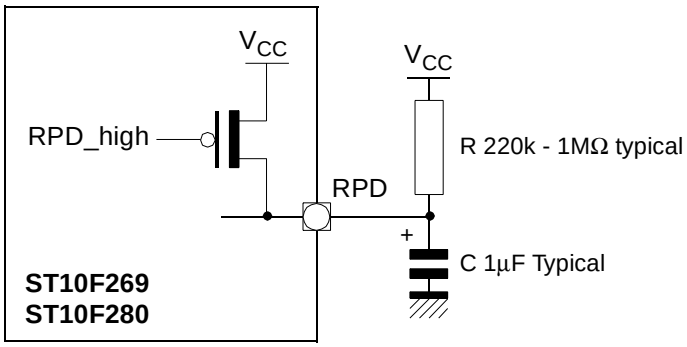
The capacitor shall be sized so that the discharge time of this capacitor into the ST10 RPD pin is:

Longer than the oscillator start-up time and PLL synchronisation time,

Shorter than the power-on reset time (after Vcc reached 4.5v), to avoid power-on reset in synchronous mode after a short supply breakdown.

Typical values are 200KΩ to 1MΩ for the resistor and 1µF for the capacitor.

Figure 10 : External RC Circuit on RPD pin for exiting powerdown mode with external interrupt



External RC circuit on RPD pin

RPD-high: driven when interruptible mode is selected & circuit not under reset & circuit not in power-down

Note: To compute the value of the component, refer to the relevant product data sheet (ST10F269, ST10F280).

10 - APPLICATION NOTE VERSION INFORMATION

10.1 - Revision of 5th of February 2001

This is the first version of AN1334.

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